REMARKS/ARGUMENTS

Claims 1-21 are pending in the application. Claims 5 and 17 have been amended to comply with the Examiner's suggestions and to add clarity.

The Examiner declared the oath and declaration defective. An Application Data Sheet has been submitted concurrent with this office action. A copy of the defective oath and declaration is enclosed.

The Examiner has objected to the drawings as not showing the features in claims 11 and 12. Figure 3 has been added listing examples of zeroing instructions. Figure 3 is identical in content to the table shown on page 5 of the specification, thus adding no new matter.

The Examiner has objected to the title as being non-descriptive. The title has been amended.

Claims 5 and 17 were rejected under 35 U.S.C. §112, second paragraph as being indefinite. Claims 17 and 19-20 were rejected under 35 U.S.C. §102(b) as being anticipated by Smith et al., U.S. Patent No. 5,367,651 (hereinafter "Smith"). Claims 18 and 21 were rejected under 35 U.S.C. §103(a) as being unpatentable over Smith in view of Rotenburg et al., Trace Cache: A Low Latency Approach to High Bandwidth Instruction Fetching (hereinafter "Rotenburg"). Claims 1, 2, 9-12, 14, and 16 were rejected under 35 U.S.C. §103(a) as being unpatentable over Smith in view of Alpha Architecture Handbook (hereinafter "Alpha") in further view of Wu, U.S. Patent No. 6,668,372 (hereinafter "Wu") in further view of Colwell et al., U.S. Patent No. 5,524,262 (hereinafter "Colwell"). Claims 3-8, 13, and 15 were rejected under 35 U.S.C. §103(a) as being unpatentable over Smith in view of Alpha, Wu, and Colwell in further view of Rotenburg.

Claim Rejections under 35 U.S.C. §112

Claims 5 and 17 were rejected under 35 U.S.C. §112, second paragraph as being indefinite. The claims have been amended to comply with the Examiner's suggestions.

Claim Rejections under 35 U.S.C. §102

Claims 17 and 19-20 were rejected under 35 U.S.C. §102(b) as being anticipated by Smith. Smith discloses integrating register allocation, instruction scheduling, instruction combining, and loop unrolling.

The applicant respectfully traverses these rejections, in part, because Smith fails to teach or suggest modifying said subsequent instruction with a pointer to a physical zero register which reads as a zero value, as called for in claim 17 as amended. The office action states as much on page 6. Therefore, claim 17 is not anticipated by Smith for at least these reasons. Applicant further respectfully submits that claims 19-20 are allowable as depending from the allowable base claims 17.

Based on the arguments above, reconsideration and withdrawal of the rejection of claims 17 and 19-20 under 35 U.S.C. §102(b) is respectfully requested.

Claim Rejections under 35 U.S.C. §103

Claims 18 and 21 were rejected under 35 U.S.C. §103(a) as being unpatentable over Smith in view of Rotenburg. Rotenburg does not teach or disclose modifying said subsequent instruction with a pointer to a physical zero register which reads as a zero value, nor does the office action claim such. Therefore claims 18 and 21 are allowable as depending from the allowable base claim 17.

Claims 1, 2, 9-12, 14, and 16 were rejected under 35 U.S.C. §103(a) as being 49524 2.DOC

unpatentable over Smith in view of Alpha in further view of Wu in further view of Colwell. Further, claims 3-8, 13, and 15 were rejected under 35 U.S.C. §103(a) as being unpatentable over Smith in view of Alpha, Wu, and Colwell in further view of Rotenburg.

It should be noted that U.S. Patent No. 6,668,372 to Wu was issued on December 23, 2003, having been filed on October 13, 1999. The present application was filed on December 28, 2000. Thus, in view of the above, Wu qualifies as prior art under 35 U.S.C. §102(e).

35 U.S.C. §103(c) states:

Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

Wu and the pending application are both assigned to Intel Corporation. Applicants submit that the present application and Wu were, at the time the claimed invention was made, assigned to Intel Corporation. Therefore, Applicants submit that Wu may not be used as a prior art reference per 35 U.S.C. §103(c). Accordingly, the rejection of claims 1-16 citing Wu should be withdrawn.

For all the above reasons, the Applicant respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application.

The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. §1.16 or §1.17 to Deposit Account No. 11-0600.

Respectfully submitted,

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Dated: April 29, 2004

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Application No.: 09/752,243 Amendment Dated: April 29, 2004 Reply to Office Action of January 29, 2004

ANNOTATED SHEET SHOWING CHANGES



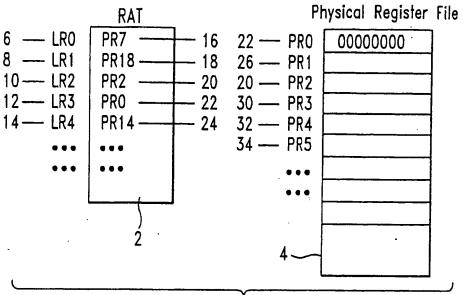


FIG. 1

A. ADD r1, r2, r3	B. STORE [r5], r1	C. XOR r1, r1, r1] 36
D . ADD r1, r5, r1	E. SUB r2, r1, r4	F. LOAD r5, [r2]	38
G. SUB r4, r4, r4	H. XOR r6, r6, r6	l. ADD r4, r4, 0x1234	- - 40

FIG. 2A (Prior Art)

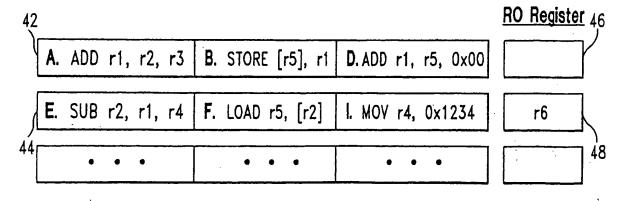


FIG. 2B